REMARKS

Examiner Berezny is thanked for his examination of the subject Patent Application. The Specification and Claims have been carefully reviewed with respect to the cited prior art, the Claim has been amended and is considered to be in condition for Allowance.

The Applicants wish to briefly point out that despite the apparent similarities to the cited prior there are important differences which form the novelty of this application.

Damascene and dual damascene processing have been part of the industry's tools for many years and the basic prior art is well known. Illustrations of the prior art are available, especially shown in the Application, Figures 1a through 1f. And again in Figures 1 through 3 of Zhou et al (US 6,358,842) which is cited by the Examiner. These figures of a dual damascene process are usually shown as a stack comprising a substrate, a metal pattern on the substrate, a first passivation layer, a first dielectric layer, an etch stop layer, a second passivation layer and a capping layer. A photoresist layer is usually shown as part of the process of transforming that stack into a deposited metal wiring pattern within the dielectric layers. But this is not the inventive portion of the instant application. This is the context in which the instant invention is found. Albeit, the same can be said for Zhou et al (US 6,358,842) which is cited by the Examiner. Like Zhou et al., the Applicants have discovered another novel way of solving the same or similar problematic defect that occurs when the damascene dielectric is a low-K dielectric, the damascene metal is copper and when conventional photoresist and etching fabrication processes are used. This topic as well as discussion of other cited art is detailed below in the particular arguments seeking reconsideration of particular rejections.

Items 1 & 2

Elections/Restrictions

The Applicants have elected claims 1 - 30 for their invention, namely a method to solve the problems of poisoning in low-k dielectric damascene processes.

Items 3, 4, 5 & 6

35 USC §112 Claims Rejection

Item 4

Reconsideration of the rejection of Claims 13 -30 under 35 USC §112 as having limitations with insufficient antecedent basis is requested based on the following amendment.

Claim 13, has been amended starting on page 27, line 1 to read:

> "A method to solve via poisoning for insulative porous low-k materials in a dual damascene structure comprising the steps of:

which now provides the antecedent for "...said dual damascene structure..." found thereafter in lines 36, 51, 54 and 57.

Item 5

Reconsideration of the rejection of Claims 8 and 25 under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention is requested based on the following amendment.

Claims 8 and 25 have been amended to remove the inclusive "and" and they now read with the alternative "or".

Item 6

Reconsideration of the rejection of Claims 10 and 28 under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention is requested based on the following amendment.

Claims 10 and 28 have been amended to remove the inclusive "and" and they now read with the alternative "or".

Item 7

Specification

The specification has been corrected to refer to a "trench (270)" in the specification at page 19, line 12, in order to remove the objection.

Item 8 & 9

35 USC § 102 Claims Rejection

Reconsideration of the rejection of Claims 1, 3-5, 7-10, 12-16, 18-20, 22, 25-26, 28 and 30 under 35 USC §102(e) as being anticipated by Zhou et al (6,358,842) is requested based on the following arguments:

The Examiner presents the rejection argument as follows:

> Zhou teaches a method to solve via poisoning for insulative porous low-k materials, see abstract, comprising the steps of: providing a silicon substrate, col.3, ln. 55-57, having a silicon nitride passivation layer with a thickness of 30-1000 Angstroms, col.4, ln.12-15, formed over a first metal layer formed on said substrate; fig.4, el.50, 58, and 54, forming a first insulative layer, with a thickness of 2000-100000 Angstroms, col.4, ln.49-52, over said substrate; el.62, forming a silicon nitride etch-stop layer, col.4, ln.60-63, with a thickness of 30-1000 Angstroms, col.4, ln.65-67, over said first insulative layer; el.66, forming a second insulative layer, with a thickness of 2000 to 100000 Angstroms, col.5, ln.34-37, over said etch-stop layer; el.70, forming a first photoresist layer over said second insulative layer and patterning said photoresist to form a first photoresist mask having a hole pattern; fig.5, el.78, etching said first and second

insulative layers, including said etch-stop layer through said hole pattern to form a hole reaching said passivation layer; fig.5, removing said first photoresist mask; *forming a low-k protection layer over said substrate, including in said hole opening; fig.6, el.82*, forming a second photoresist layer over said substrate, including said hole opening and patterning said second photoresist to form a second photoresist mask having a trench pattern; fig.9, etching said second insulative layer through said trench pattern in said second photoresist mask to form a trench in said second insulative layer, thus completing the forming of said dual damascene structure in said substrate; fig.1 0, *removing said second photoresist mask; fig.11, removing said low-k protection layer from over said substrate and from the bottom of said hole opening and thereby exposing underlying said passivation layer while leaving said low-k protection layer on the vertical sides of said hole opening;* fig.6, el.82, removing said passivation layer from said bottom of said hole opening, thereby exposing underlying said first metal layer; fig.7, el. 82, 86, forming a barrier layer over said substrate, including in said dual damascene structure; fig.13, el.1 04, depositing a second metal, such as copper, over said barrier layer in said dual damascene structure; fig.13, el.106, and performing chemical mechanical polishing (CMP) to complete the forming of said dual damascene structure, col.8, ln.6-63. **Further, Zhou teaches forming a low-k protection layer comprises Si02, SiN, SiC and SiNCG, col.6, ln.18-25, wherein said low-k protection layer has a thickness between about 20 to 1000 A,. col.6, ln.46-50,** and wherein said barrier layer comprises Ta,. Ti, TaN, TiSIN, TaSiN,. WN, col.8, ln. 58-58.

The Applicants agree with the Examiner that the underlined passages represent a prior art description of a semiconductor damascene process. They further agree that the passages in italics represent areas in which Zhou et al. have made their inventive contribution but suggest that it is not accurate. However, the Applicants disagree with the Examiner in two ways. Firstly, the passage in bold print is in error. The compounds **Si02, SiN, SiC and SiNC** are **not** found discussed anywhere in the specification of Zhou et al. let alone in column 6, lines 18-25. Secondly, the italicized passages do not describe the instant invention.

At the point in the damascene process when the first etching is complete, Zhou et al. strip the photoresist using a sulfur base compound and in doing so **simultaneously deposit a sulfur-containing layer** on the sidewall of the via. Further in the damascene process when the second etching is complete, Zhou et

al. again strip the photoresist using a sulfur base compound and in doing so **simultaneously deposit a second sulfur-containing layer** on all the exposed low-k dielectric surfaces. This double sulfur containing layer forms their low-K protection layer. Subsequently, a barrier layer of Ta, TaN, TiN, or WN is deposited as conventionally used for damascene copper deposition.

By contrast, but within the same or similar context, the Applicants provide a low-K protective lining to prevent poisoning the copper inlay. When stripping of the first photoresist is required, the Applicants do **not** make use of a simultaneous operation, but do require two separate operations which they can control separately. First, they use oxygen plasma etching to assure complete stripping of the photoresist. Then they deposit a single thin (50 to 400 Angstrom) film of **Si02, SiN, SiC or SiNC** on the sidewalls of the via. Although there is a subsequent second photoresist operation, there is only one protective layer deposited. A barrier layer of (note a larger family than that of Zhou et al.) Ta, Ti, TaN, TiSIN, TaSiN, or WN is deposited.

Although the bulk of the description of both Zhou et al. and the instant application is in the context of prior art damascene processes both Zhou et al. and the instant application disclose completely different methods of precluding poisoning of copper deposited in low-K dielectric trenches and via holes. While Zhou et al. uses a **simultaneous** strip and deposit, the instant invention uses **separately** controlled operations. While Zhou et al. provides **two** protective coatings, the instant invention provides just **one**. While Zhou et al. deposit a

sulfur containing layer, the instant invention deposits a **silicon** containing layer.

The above discussion has not dealt with the other possibly major or minor differences between the instant invention and Zhou et al. such as thickness of materials and recipes of etching compounds.

Item 10, 11 & 12

35 USC § 103(a) Claims Rejection

Reconsideration of the rejection of Claims 11, 23-24, 27, and 29 under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. as applied to claims 1, 3-5, 7-10, 12-16, 18-20, 22, 25-26, 28 and 30 above, and further in view of Lin (US 6,140,220) is requested based on the following arguments:

Item 11

The Examiner suggests the following:

> Zhou appears, not to specify the thickness of the barrier film, nor the etch chemistry used to etch the first and second insulators, the etch stop layer, and the protective layer. Lin teaches forming a barrier layer comprising Ta or TaN, having a thickness of 100-2000 Angstroms, col.4, ln.18-23. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Lin with Zhou to use a barrier layer of the same material with a thickness used by Lin to prevent via poisoning, thereby reducing contamination of the interconnect structure.

The Applicants reply by noting that the objects of Lin are:

> A further object on the invention has been that said dual damascene structure provide **low via hole resistance** between wiring levels without sacrificing the effectiveness of the diffusion barrier.
>
> These objects have been achieved by means a structure in which the via hole is first lined with a **layer of silicon nitride** prior to adding the diffusion barrier and copper. This allows use of **a barrier layer that is thinner than normal** (since the silicon nitride liner is an effective diffusion barrier) **so that more copper** may be included in the via hole, resulting in an improved conductance of the via.

Despite the presence of a silicon nitride layer, Lin still requires the use of a barrier layer of 100 to 2000 Angstroms of Ta or TaN. By contrast a much thinner 30 to 500 Angstrom (~25%) layer is used in the instant invention.

Item 12

The Examiner observes:

> Further, **Lin teaches using etchant gases containing CHF3 and CF4 mixed with oxygen.** It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the well known teachings of using fluorocarbon and oxygen etch chemistry, as exemplified by Lin, to etch the materials of the first and second insulator, the etch stop, and the protective layer, in order to etch these materials quickly and under control, while also producing volatile exhaust gases that helps keep the wafer and chamber cleaner from contaminants. In addition, it is well known in the art to employ inert carrier gasses, such as Ar and Nitrogen. It would have been obvious to one of ordinary skill in the art at the time of the invention to use Ar and nitrogen to control the etchant concentration in the chamber, thereby better controlling the etch rate of the material being etched, thereby reducing the chances of over-etching the material.

The Applicants respond by noting that in Lin's specification, CHF3 and CF4 mixed with oxygen is applied to items 21, 71, 72 and 92, which are respectively found at column 1, line 32, column 4, line 4, column 3, line 38 and column 4, line 4 defined respectively as silicon oxide, silicon nitride, silicon oxide and silicon nitride. Silicon oxide and silicon nitride are not low-K dielectrics. Furthermore, Lin's only use of the word "low" is to modify the words "resistance", "selectivity" and "pressure". Therefore there are **no** low-K dielectrics in Lin. Lin does **not** teach low-K dielectrics. Lin does **not teach etching** of low-K dielectrics. CHF_3 (or CF_4) plus oxygen is used to etch silicon oxide and silicon nitride.

Furthermore, C_2F_6, C_4F_8, Ar, N_2 and O_2 are the components of a recipe the Applicants use to etch low-K dielectrics. It is a recipe that is not of Lin and most likely would be of no use to Lin.

Item 13

35 USC § 103(a) Claims Rejection

Reconsideration of the rejection of Claims 2, 6, 17 and 21 under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. as applied to claims 1, 3-5, 7-10, 12-16, 18-20, 22, 25-26, 28 and 30 above, and further in view of Eissa et al. (US 2002/0127876) is requested based on the following arguments:

The Examiner observes:

> Zhou appears not to specify the k value of the low-k dielectric used in the first and/or the second dielectric. **Eissa teaches the use of a low-k dielectric** in a copper dual damascene interconnect structure having a k value between 2.0 and 3.0, page 1, par. [0010]. It would have been obvious to one of ordinary skill in the art at the time of the invention to select a low-k dielectric having a k-value between 2.0 and 3.0 in an interconnect structure having copper, in order to reduce the parasitic capacitance of the interconnect thereby reducing the RC constant and increasing the speed and performance of the devices.

The Applicants reply by asserting that they are using a low-K dielectric with the low resistance conductor copper for the obvious reason of achieving an increase in speed and performance due to the well known approach of reducing the RC time constant. It is what almost everyone practicing the art is doing. Eissa et al. does not teach anything new in this regard. The Applicants, as well as the current and prior art practitioners, are using commercial low-K dielectric products like FLARE, SiLK, etc. which are advertised to have low dielectric constant. Eissa et al. have merely discovered another way to control the generation of defects of poisoning copper damascene in low-K dielectrics, which the Applicants do not employ.

CONCLUSION

It is respectfully suggested that these various references cannot be combined without reference to applicants' own invention. It is believed that independent claims 1 and 13, and hence claims dependent from claim 1, and claims dependent from claim 13, as amended, are allowable, and we therefore request respectfully that Examiner Berezy reconsider these rejections in view of these arguments and the amendments and allow claims 1 through 30

We have reviewed the related art references made of record and agree with the Examiner that none of these suggest the present claimed invention.

In light of the above arguments, it is suggested that the specification now adequately describes the invention and that the Claims now clearly distinguish the invention from the prior art. All claims are therefore believed to be in condition for allowance.

Allowance of all claims is therefore respectfully requested.

It is request that should Examiner Berenzy not find that the Claims are now Allowable that the Examiner call the undersigned attorney at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

Stephen B Ackerman, Reg. No. 37,761

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In the Sp cification

Next, second photoresist layer (260) is formed over the substrate, including the opening formed in the previous step, and patterned with the image of a line to form a second photoresist mask with a trench [(280)] (270) as shown in Fig. 2d. The line pattern is next transferred from the second photoresist mask into the second dielectric layer by etching and stopping on etch-stop layer (225). This is accomplished by etching the second low-k dielectric layer by using a recipe comprising C_2F_6, C_4F_8, Ar, N_2 and O_2 . It will be noted that the low-k protection layer (250) is also removed from the bottom of hole opening (245) thereby exposing the underlying passivation layer, while leaving the protective layer on the vertical walls of the hole, as seen in Fig. 2e. Then passivation layer (215) is removed from the bottom of the hole opening using a recipe comprising C_2F_6, C_4F_8, Ar, N_2 and O_2 and exposing the underlying first metal layer (210), as shown in Fig. 2f. This is followed by the removal of the second photoresist layer, hence completing the forming of a damascene structure having a composite hole (245) and line (270) pattern as shown in Fig. 2f.

In the Claims

10. (AMENDED ONCE) The method of claim 1, wherein said barrier layer comprises Ta, Ti, TaN, TiSiN, TaSiN, or WN.

13. (AMENDED ONCE) A method to solve via poisoning for insulative porous low-k materials in a dual damascene structure comprising the steps of:

providing a substrate having a passivation layer formed over a first metal layer formed on said substrate;

forming a first insulative layer over said substrate;

forming an etch-stop layer over said first insulative layer;

forming a second insulative layer over said etch-stop layer;

forming a first photoresist layer over said second insulative layer and patterning said photoresist to form a first photoresist mask having a hole pattern;

etching said first and second insulative layers, including said etch-stop layer through said hole pattern to form a hole reaching said passivation layer;

removing said first photoresist mask;

forming a low-k protection layer over said substrate, including in said hole opening;

forming a second photoresist layer over said substrate, including said hole opening and patterning said second photoresist to form a second photoresist mask having a trench pattern; .

etching said second insulative layer through said trench pattern in said second photoresist mask to form, a trench in said second insulative layer, thus completing the forming of said dual damascene structure in said substrate;

removing said second photoresist mask;

removing said low-k protection layer from over said substrate and from the bottom of said hole opening and thereby exposing underlying said passivation layer while leaving said low-k protection layer on the vertical sides of said hole opening;

removing said passivation layer from said bottom of said hole opening, thereby exposing underlying said first metal layer;

forming a barrier layer over said substrate, including in said dual damascene structure;

depositing a second metal over said barrier layer in said dual damascene structure; and

performing chemical mechanical polishing (CMP) to complete the forming of said dual damascene structure.

28. (AMENDED ONCE) The method of claim 13, wherein said barrier layer comprises Ta, Ti, TaN, TiSiN, TaSiN, or WN.